REMARKS

Claims 7 and 12 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The claims have been amended in a readily apparent manner to overcome this rejection. Withdrawal is respectfully requested.

Claims 1-3, 8, 9, 13 and 14 stand rejected under 35 U.S.C. §102(b) as being anticipated by Koeda "Operating System of the VX/VPP300/VPP700 Series of Vector-Parallel Supercomputer Systems." Claim 1 has been amended to incorporate the features of claims 4 and 5, which have been canceled, and claims 13 and 14 have been amended in a similar manner. Claim 8 has been amended to incorporate the features of claims 10 and 11, which have also been canceled. Since claims 4, 5, 10 and 11 have not been rejected under §102(b), this rejection is now believed to have been overcome. Withdrawal is respectfully requested.

Claims 4-7 and 10-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Koeda. The features of these claims have been incorporated into their respective dependent claims 1 and 8. Accordingly, Applicants respectfully traverse this rejection with respect to amended claims 1, 8 and 12.

The claimed invention discloses assigning each parallel process to a processor in each time slot according to one of the throughput-first policy and the turnaround-first policy. While the turnaround-first policy is selected, no batch processing is assigned even when a free time slot exists. This makes it possible to guarantee the turnaround time. In addition, the total amount of time that each parallel program occupies each processor does not depend on the presence of free time slots. Accordingly, in the case where customers are billed according to the processing time in processors, the customers are billed the same amount of fee as long as

executed parallel programs have the same content. It should be noted that interactive processing can be performed in free time slots.

By contrast, Koeda teaches setting the distribution of CPU use between interactive processing and batch processing, and does not disclose or suggest that batch processing is not assigned even when a free time slot exists. In addition, Koeda only teaches a Simplex mode that does not allow a job to be executed while another job is performed in the Simplex mode. The Simplex mode does not guarantee the turnaround time. For these reasons, claims 1-3, 6-8, 13 and 14 are allowable over Koeda.

Claims 7 and 12 describe simultaneously executing parallel processes at a time allocation ratio in a system where processors are separately installed in a plurality of nodes. However, the nodes individually manage execution of processors, which causes a time lag in processing timing. Therefore, the coordination controller notifies nodes that will execute parallel processes, of a start time of the processes when the start time comes, so as to synchronize the start timing. This feature is supported in Fig. 16.

By contrast, Koeda teaches a standalone parallel operating system (FIG. 1), in which a PM collectively manages the execution of processes. In other words, Koeda does not disclose or suggest simultaneously executing parallel processes in a system where each node manages execution of parallel processes in cooperation with each other. Claims 7 and 12 are allowable for this reason.

For all of the above reasons, Applicants request reconsideration and allowance of the claimed invention. Should the Examiner be of the opinion that a telephone conference would aid in the prosecution of the application, or that outstanding issues exist, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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December 3, 2007

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